REMARKS

This Preliminary Amendment is filed in order to facilitate processing of the above identified application and responds to the Office Action dated November 28, 2005 in which the Examiner rejected claims 1-3 under 35 U.S.C. §102(b) and rejected claim 4 under 35 U.S.C. §103.

As indicated above, Claim 1 has been amended to make explicit what is implicit in the claim. The amendment is unrelated to a statutory requirement for patentability.

Claim 1 claims a memory device comprising a memory unit and an arbiter. The arbiter controls the memory unit while arbitrating for a bus access request from a plurality of units outside the memory unit. When a second bus access request takes place before an access to the memory unit that corresponds to a first bus access request has been completed, the arbiter performs activation of the memory unit that corresponds to the second bus access request in parallel with writing or reading data to/from the memory unit that corresponds to the first bus access request after an address signal is input to the memory unit.

Through the structure of the claimed invention having an arbiter which a) arbitrates for a memory bus access request from a plurality of units outside the memory unit and b) activates the memory unit in parallel with writing/reading of another bus access request, as claimed in claim 1, the claimed invention provides a memory device which prevents reduced processing performance of the entire system by reducing the number cycles required to access a memory. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1-3 were rejected under 35 U.S.C. §102(b) as being anticipated by *Dreibelbis et al* (U.S. Patent No. 5,875,470).

Dreibelbis et al. appears to disclose a multi-port multi-bank memory architected to enable manufacture of the memory in a single DRAM chip having a plurality of input/output ports and being capable of handling a large number of accesses in parallel. (col. 1, lines 8-12). An architecture for a semiconductor chip containing multiple bidirectional ports supporting a plurality of independent DRAM banks all packaged in the single chip. Access requests are supported from plural processors, or plural execution units, connected to different ports of the chip. Simultaneously independent accesses may be made in the separate DRAM banks within the chip without causing conflict among parallel requests to different sections of the memory within the chip. Any conflict among parallel requests to the same section of the memory may be resolved within the chip. This invention is not concerned with access conflict resolution made outside of the memory chip. (col. 1, lines 40-51, emphasis added) The chip structure shown in FIGS. 1A and 1B is logically divided into distinct parts, including DRAM storage parts shown in FIG. 1A, and an input/output part shown in FIG. 1B. The storage part in FIG. 1A comprises four DRAM memory sections 1, 2, 3 and 4. Each memory section contains four DRAM storage banks connected to one data bus 5. The four storage sections 1, 2, 3, 4 each have a respective data bus 5-1, 5-2, 5-3, 5-4. The four sections therefore have a total of 16 DRAM banks 1.1 through 4.4. Further, each DRAM bank is connected to a respective one of sixteen address buses 11-1 through 14-4, which are connected to a bank address control 10 within the chip. Bank address control 10 may receive all memory addresses requested by all processors wanting to access

data in any of the 16 banks in memory sections 1, 2, 3 and 4. Control 10 may be simultaneously providing plural addresses on buses 11-1 through 11-4 for simultaneously selecting the drivers for one of matrix rows in multiple banks. (Col. 4, line 54 through col. 5, line 5)

Thus, *Dreibelbis et al.* merely discloses a control 10 which simultaneously provides plural addresses on buses for simultaneously selecting the drivers for one of the matrix rows in multiple banks (col. 5, lines 2-5). Nothing under *Dreibelbis et al.* shows, teaches or suggests an arbiter forming activation of a memory unit that corresponds to a second bus accessed request in parallel with writing/reading of data to/from a memory unit that corresponds to a first bus access request after an address signal is input to the memory unit as claimed in claim 1. Rather, *Dreibelbis et al.* merely discloses a control 10 which simultaneously provides addresses for simultaneously selecting drivers for one of the matrix rows in multiple banks.

Also, *Dreibelbis et al.* merely discloses access requests from processors made inside a memory chip and is not concerned with access conflict resolution made outside of the memory chip (column 1, lines 50-52). Thus nothing in *Dreibelbis et al.* shows, teaches or suggests an arbiter controlling a memory unit while arbitrating for memory bus accessed requests from a plurality of units outside the memory unit as claimed in claim 1. Rather, *Dreibelbis et al.* teaches away from the claimed invention and states that it is not concerned with access conflict resolution made outside of the memory chip.

Since nothing in *Dreibelbis et al.* shows, teaches or suggests an arbiter which arbitrates for memory bus access requests from a plurality of units outside the memory unit and which activates a memory unit for a second bus access request in

parallel with writing/reading data to/from the memory unit that corresponds to a first bus access request after an address signal is input to the memory unit, as claimed in claim 1, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2-3 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-3 would not have been anticipated by *Dreibelbis et al* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2-3 under 35 U.S.C. §102(b).

Claim 4 was rejected under 35 U.S.C. §103 as being unpatentable over *Dreibelbis et al* and further in view of *Masuoka et al* (U.S. Patent No. 6,472,714).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claim has been reviewed in light of the Office Action, and for reasons which will be set forth below, applicants respectfully request the Examiner withdraws the rejection to the claim and allows the claim to issue.

As discussed above, since nothing in *Dreibelbis et al* shows, teaches or suggests the primary feature as claimed in claim 1, applicants respectfully submit that the combination of the primary reference with the secondary reference to *Masuoka et al* would not overcome the deficiencies of the primary reference. Therefore, applicants respectfully request the Examiner withdraws the rejection to claim 4 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for

allowance, Applicants respectfully request the Examiner enters this Amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

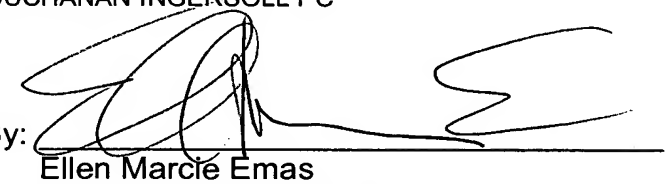
In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

Date: February 27, 2006

By: 

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